Please amend claims 29, 36, 64 and 71, as follows. The "marked-up" version of the amended claims are provided in the APPENDIX attached hereafter.

29. (Twice Amended) A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode, a drain electrode and a data line connected to the source electrode on the semiconductor pattern, wherein the gate insulating layer, the semiconductor pattern and the data wire are patterned in a single photolithography step;

forming color filters made of photosensitive material, the color filters covering data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters.

36. (Amended) The method of claim 35, wherein the gate wire and the data wire are patterned through a photolithography process including only exposure and development steps.

64. (Amended) A thin film transistor array panel for a liquid crystal display, comprising:

a plurality of gate lines formed on an insulating substrate;

a gate insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines;

an amorphous silicon layer formed under the entire data lines;

an ohmic contact layer interposed between the data lines and the amorphous silicon layer;

an array of thin film transistors, each transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode;

a plurality of color filters formed over the gate insulating layer, the color filters overlapping the data lines at last in part; and

a plurality of pixel electrodes formed on the color filters, each pixel electrode electrically connected to the drain electrode.

71. (Amended) A thin film transistor array panel for liquid crystal display, comprising:

a plurality of gate lines formed on an insulating substrate;

a first insulating layer covering the gate lines;

a plurality of data lines intersecting the gate lines;

an amorphous silicon layer formed under the entire data lines;

an ohmic contact layer interposed between the data lines and the amorphous silicon layer;

an array of thin film transistors, each transistor including a gate electrode connected to the gate line, a source electrode connected to the data line, and a drain electrode;

a second insulating layer formed at least on the data lines, the second insulating layer contacting a portion of the amorphous silicon layer exposed between the source electrode and the

drain electrode; and

a plurality of pixel electrodes formed on the second insulating layer, each pixel electrode electrically connected to the drain electrode.

Please add new claims 75-80, as follows.

75. (New) The thin film transistor array panel of claim 71, wherein said second insulating layer has a contact hole exposing a portion of one of the data lines near an end of the one of the data lines.

76. (New) The thin film transistor array panel of claim 75, further comprising a redundant data pad contacting the exposed portion of the data lines through the contact hole.

77. (New) The thin film transistor array panel of claim 75, wherein the redundant data pad is made of the same layer as the pixel electrodes.

78. (New) The thin film transistor array panel of claim 71, wherein said first insulating layer and said second insulating layer has a contact hole exposing a portion of one of the gate lines near an end of the one of the gate lines.

79. (New) The thin film transistor array panel of claim 78, further comprising a redundant gate pad contacting the exposed portion of the gate lines through the contact hole.